REMARKS

Applicants have studied the Office Action dated June 29, 2007, and have made amendments to the claims. In particular, claims 1-2, 15, and 19 have been. No new matter has been added. Claims 1-7 and 10-24 are pending in the application. Reconsideration and allowance of the pending claims in view of the following remarks are respectfully requested. Applicants submit that the present response places the application in condition for allowance. In the Office Action, the Examiner:

- rejected claims 1-26 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No 5,826,081 to Zolnowsky in view of U.S. Patent No5,615,374 to Sadoi et al.

Claim Rejections - 35 USC §103

As noted above, the Examiner rejected claims 1-26 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No 5,826,081 to Zolnowsky in view of U.S. Patent No5,615,374 to Sadoi et al.

Zolnowsky discloses a process scheduler for a multiprocessor system for real time applications. Each processor in Zolnowsky has its own queue and a dispatcher so that the system can maintain a dispatch queue for each processor and a separate global dispatch queue for unbound higher priority real time threads. Zolnowsky further discloses that each queue has a separate schedule lock associated with it to protect scheduling operations. A processor is allowed to place a new thread on the global high priority real time queue, the processor's own queue, or any other processor's queue. A processor's dispatcher can select a thread for execution from the global real time queue, a processor's own queue, or another processor's queue as a candidate thread to execute, based upon priority variables associated with each queue. Zolnowsky also discloses that the examination of the priorities on queues for thread selection does not require any schedule locks and miscommunication is prevented by using a suitable synchronization algorithm.

Zolnowsky also teaches that when a candidate thread is selected for execution, the processor notifies other processors of its selection and proceeds to verify against threads in the global real time queue and the processor's own dispatch queue to select the highest priority runnable thread in the system. Thus, system disclosed by Zolnowsky allows the dispatcher to prevent race conditions and minimize lock contention while assuring that high-priority threads are dispatched as quickly as possible.

The presently claimed invention, on the other hand, now more clearly recites

> *An exclusion controller which allows an information processing unit to acquire a contended resource to the exclusion of other information processing units, the exclusion controller comprising:*
>
> *a storage area including*
>
> *i) a prioritized information processing unit information storage area for storing information for identifying a prioritized information processing unit that is to execute writes for acquiring a contended resource by using normal write instructions;*
>
> *ii) a prioritized exclusion right information storage area for storing information indicating whether the prioritized information processing unit is trying to acquire the contended resource; and*
>
> *iii) a non-prioritized exclusion right information storage area for storing non-prioritized exclusion right information that indicates whether a non-prioritized exclusion right has been acquired by a non-prioritized information processing unit,*
>
> *a plurality of non-prioritized information processing units mutually exclusively acquiring a non-prioritized exclusion right by a first process using the information in the non-prioritized exclusion right information storage area to determine that the non-prioritized exclusion right information has not yet been stored, the non-prioritized exclusion right indicating a candidate for acquiring the contended resource, the first process executing writes by using compare-and-swap instructions; and*
>
> *a prioritized information processing unit identified by the prioritized information processing unit information storage area acquiring the contended resource by a second process to the exclusion of the non-prioritized information processing unit having acquired the non-prioritized exclusion right, the exclusion being determined from the non-prioritized exclusion right information storage area, updating the information in the prioritized exclusion right information storage area to indicate that the prioritized information processing unit is trying to acquire the contended resource, the second process executing writes by using normal write instructions.*

The Examiner, on page 2 of the present Office Action states that Zolnowsky teaches:

> *An exclusion controller which allows an information processing unit to acquire a contended resource to the exclusion of other information processing units, the exclusion controller comprising:*
> *a plurality of non-prioritized information processing units mutually exclusively acquiring a non-prioritized exclusion right by a first process, the non-prioritized exclusion right indicating a candidate for acquiring the contended resource*

The Examiner further states "Figure 5 illustrates said controller controlling high priority queue 501 that allows the selected thread to access shared resource 503, excluding other threads. These steps are shown in figure 7, steps 701 and 702, Col. 8, lines 14-18". Col. 8, lines 14-18 merely state:

> Referring now to FIG. 7, if the real time queue has a higher priority thread than its own dispatch queue at decision block 701, the processor dispatcher acquires a lock for the real time queue and takes a highest priority thread at step 702 from the real time queue such as queue 404 of FIG. 4 and proceeds to execute the thread.

This is not the same as the claim element in question. The claim element in question recites "…

a plurality of non-prioritized information processing units mutually exclusively acquiring a non-prioritized exclusion right by a first process, the non-prioritized exclusion right indicating a candidate for acquiring the contended resource…". In other words, the contended resource is not acquired by the non-prioritized information processing unit, the non-prioritized information processing unit only becomes a candidate for acquiring the contended resource. Zolnowsky, on the other hand, states that the "processor dispatcher acquires a lock for the real time queue and takes a highest priority thread at step 702 from the real time queue such as queue 404 of FIG. 4 and proceeds to execute the thread". In other words, the resource is acquired. Also, Zolnowsky does not distinguish between a non-prioritized information processing unit and a prioritized information processing unit. Zolnowsky is completely silent on this aspect of the presently claimed invention. Accordingly, the presently claimed invention distinguishes over Zolnowsky for at least these reasons.

Furthermore, claim 1 has been amended to more clearly recite

> *[…]*
> *the exclusion controller comprising:*
> *a storage area including*
> *i) a prioritized information processing unit information storage area for storing information for identifying a prioritized information processing unit that is to execute writes for acquiring a contended resource by using normal write instructions;*
> *ii) a prioritized exclusion right information storage area for storing information indicating whether the prioritized information processing unit is trying to acquire the contended resource; and*
> *iii) a non-prioritized exclusion right information storage area for storing non-prioritized exclusion right information that indicates whether a non-prioritized exclusion right has been acquired by a non-prioritized information processing unit,*
> *a plurality of non-prioritized information processing units mutually exclusively acquiring a non-prioritized exclusion right by a first process using the information in the non-prioritized exclusion right information storage area to determine that the non-prioritized exclusion right information has not yet been stored, the non-prioritized exclusion right indicating a candidate for acquiring the contended resource, the first process executing writes by using compare-and-swap instructions; and*
> *a prioritized information processing unit identified by the prioritized information processing unit information storage area acquiring the contended resource by a second process to the exclusion of the non-prioritized information processing unit having acquired the non-prioritized exclusion right, the exclusion being determined from the non-prioritized exclusion right information storage area, updating the information in the prioritized exclusion right information storage area to indicate that the prioritized information processing unit is trying to acquire the contended resource, the second process executing writes by using normal write instructions.*

Nowhere does Zolnowsky teach these elements. It should be noted that some of the language from claim 2 has been incorporated into claim 1. The Examiner states on pages 3-4 of the present Office Action with respect to claim 2 that Zolnowsky teaches:

> a prioritized exclusion right storage area for storing prioritized exclusion right information indicating that the prioritized information processing unit is trying to acquire the contended resource (Figure 4A illustrates a storage area, queue 404, associated with controller processor N (403) that stores required thread, COL. 6, lines 30 — 35); and
> a non-prioritized exclusion right storage area for storing non-prioritized exclusion right information indicating which of the plurality of non-prioritized information processing units has acquired the non-prioritized exclusion right,

> wherein each non-prioritized information processing unit executes, as the first process, a process for storing the non-prioritized exclusion right information indicating that the non-prioritized information processing unit has acquired the non-prioritized exclusion right, to the exclusion of the other non-prioritized information processing units if the non-prioritized exclusion right information has not yet stored, and the prioritized information processing unit executes, as the second process, a process for storing the prioritized exclusion right information and then reading the non-prioritized exclusion right storage area, and acquires the contended resource if the non-prioritized exclusion right information is not stored, but does not acquire the contended resource if the non-prioritized exclusion right information has already stored (Figure 4A illustrates processor 1, processor 2, as non-prioritized processing unit comprising queues such as 401 that comprises the non-prioritized threads, COL.6 , lines 30 — 52).

Col. 6, lines 30-52 merely state that:

> FIG. 4(A) shows a multiple dispatcher queue system according to a preferred embodiment of the present invention. Referring to FIG. 4(A), the multiple dispatcher queue system comprises separate dispatcher queues 401, 402, . . . , 403 for processors 1, 2, . . . , N and in addition, a global high priority real time queue 404, which is used to hold high priority real time threads. Each dispatch queue has its own scheduling lock associated with it to protect all scheduling operations so that any processor attempting to dispatch a thread from a queue needs to acquire a lock for that queue before taking the thread off the queue. Thus, lock contention is reduced in the present invention with multiple schedule locks for multiple dispatch queues in contrast to prior art schedulers wherein a single schedule lock is used for a single dispatch queue for all processors.
>
> In the preferred embodiment of FIG. 4(A), a dispatcher uses an array of dispatch queues, indexed by dispatch priority. Also, when a thread is made runnable, it is placed on a dispatch queue, typically at the end, corresponding to its dispatch priority. However, other schemes can be used for queueing instead of FIFO thread queueing. For example, LIFO (Last In First Out), SJF (Shortest Job First), SRT (Shortest Remaining Time) or other sophisticated queueing mechanism can be used depending on real time application scheduling requirements.

The Examiner is incorrectly comparing the real time queue 404 of Zolnowsky with the presently claimed "prioritized exclusion right information storage area". The real time queue 404 of Zolnowsky is "used to hold high priority real time threads". These threads are in the queue to be scheduled on a processor. The "prioritized exclusion right information storage area" of the presently claimed invention, on the other hand "stor[es] information for identifying a prioritized information processing unit that is to execute

writes for acquiring a contended resource by using normal write instructions". As can be seen, the prioritized exclusion right information storage area is not a queue for threads. In fact, the entire focus of Zolnowsky is to schedule threads where the presently claimed invention allows an information processing unit (such as a processor or a thread) to acquire a contended resource to the exclusion of other information processing units. Accordingly, the presently claimed invention distinguishes over Zolnowsky for at least these reasons as well.

Furthermore, nowhere does Zolnowsky teach a "non-prioritized exclusion right information storage area" as recited for the presently claimed invention. A "non-prioritized exclusion right information storage area" stores "non-prioritized exclusion right information that indicates whether a non-prioritized exclusion right has been acquired by a non-prioritized information processing unit". A queue 401 in Zolnowsky is associated with a particular processor and stores threads to be scheduled for execution. As can be seen, this is completely different than the above claim element. Accordingly, the presently claimed invention distinguishes over Zolnowsky for at least these reasons as well.

Claim 1 further recites "a prioritized information processing unit information storage area for storing information for identifying a prioritized information processing unit that is to execute writes for acquiring a contended resource by using normal write instructions". Nowhere does Zolnowsky teach this claim element. As discussed above, Zolnowsky does not teach a non-prioritized information processing unit that performs a first process and a prioritized information processing unit that performs a second process. Col. 6, lines 30-52 of Zolnowsky nor does anywhere else in Zolnowsky mention anything about a prioritized information processing unit and a non-prioritized information processing unit utilizing information within a non-prioritized exclusion right information storage area let alone the a prioritized information processing unit utilizing both the non-prioritized exclusion right information storage area and prioritized exclusion right information storage area.

Therefore, Zolnowsky does not teach or suggest:

> *a plurality of non-prioritized information processing units mutually exclusively acquiring a non-prioritized exclusion right by a first process using the information in the non-prioritized exclusion right information storage area to determine that the non-prioritized exclusion right information has not yet been stored, the non-prioritized exclusion right indicating a candidate for acquiring the contended resource, the first process executing writes by using compare-and-swap instructions; and*
>
> *a prioritized information processing unit identified by the prioritized information processing unit information storage area acquiring the contended resource by a second process to the exclusion of the non-prioritized information processing unit having acquired the non-prioritized exclusion right, the exclusion being determined from the non-prioritized exclusion right information storage area, updating the information in the prioritized exclusion right information storage area to indicate that the prioritized information processing unit is trying to acquire the contended resource, the second process executing writes by using normal write instructions.*

Accordingly, the presently claimed invention distinguishes over Zolnowsky for at least these reasons as well.

The Applicants agree with the Examiner that Zolnowsky does not teach "the first process executing writes using compare and swap instruction". However, the Examiner goes onto combine Zolnowsky with Sadoi stating that Sadoi teaches "using the swap and compare instruction prior to the locking of the resource by any particular CPU as illustrated in Figure 5. Step 821 illustrates writing CPU 1D into lock control by CS instruction, COL. 4, lines 45 -53. …Sadoi also teaches of a prioritized information processing unit acquiring the contended resource by a second process to the exclusion of the non-prioritized information processing unit having acquired the non-prioritized exclusion right, the second process executing writes by using normal write instructions (Figure 5 illustrates acquiring resource by writing CPU ID into lock control in step S26, COL. 5, lines 15-23."

Sadoi does not teach both a non-prioritized information processing unit and a prioritized information processing unit. In fact, where the Examiner directs the Applicants to , FIG. 5, col. 4, lines 45-53, and col. 5, lines 15-23 explicitly teach that a single CPU "attempts

to write the CPU identifier assigned thereto into the lock control information (CPU) 1 by using the compare and swap (CS) instruction". In other words, Zolnowsky does not teach a separate non-prioritized information processing unit that performs a first process executing writes by using compare-and-swap instructions and a separate prioritized information processing unit that performs executing writes by using normal write instructions. FIG. 5, col. 4, lines 45-53, and col. 5, lines 15-23 are referring to the same instance of writing the CPU identifier into the lock control information by a single CPU.

The presently claimed invention, on the other, hand recites two separate entities a non-prioritized information processing unit and a prioritized information processing unit that each perform a process the other does not. For example, the non-prioritized information processing unit that performs a first process executing writes by using compare-and-swap associated with non-prioritized exclusion right and the prioritized information processing unit that performs executing writes by using normal write instruction for indicating that that the prioritized information processing unit is trying to acquire the contended resource and for the actual acquiring of the contended resource. Accordingly, the presently claimed invention distinguishes over Zolnowsky alone and/or in combination with Sadoi for at least these reasons.

Furthermore, Sadoi merely teaches a class lock and a non-class lock. The class lock is a classified lock based on an application. There are lock control areas for respective classes, and the lock can be acquired for each of the classes. The non-class lock is a non-classified lock, and there is a single lock control area as a whole. The lock for the whole resource can be acquired. The presently claimed invention, on the other hand, now more clearly recites:

> *a storage area including*
>
> *i) a prioritized information processing unit information storage area for storing information for identifying a prioritized information processing unit that is to execute writes for acquiring a contended resource by using normal write instructions;*
>
> *ii) a prioritized exclusion right information storage area for storing information indicating whether the prioritized information processing unit is trying to acquire the contended resource; and*

> *iii) a non-prioritized exclusion right information storage area for storing non-prioritized exclusion right information that indicates whether a non-prioritized exclusion right has been acquired by a non-prioritized information processing unit,*

Nowhere does Sadoi teach these elements. Accordingly, the presently claimed invention distinguishes over Zolnowsky alone and/or in combination with Sadoi for at least these reasons.

Furthermore, the Examiner's citations of Sadoi at FIG. 5, col. 4, lines 45-53, and col. 5, lines 15-23 show that Sadoi is using the compare and swap instruction to write to the non-class lock. However, claim 1 recites:

> *a plurality of non-prioritized information processing units mutually exclusively acquiring a non-prioritized exclusion right by a first process using the information in the non-prioritized exclusion right information storage area to determine that the non-prioritized exclusion right information has not yet been stored, the non-prioritized exclusion right indicating a candidate for acquiring the contended resource, the first process executing writes by using compare-and-swap instructions; and*
>
> *a prioritized information processing unit identified by the prioritized information processing unit information storage area acquiring the contended resource by a second process to the exclusion of the non-prioritized information processing unit having acquired the non-prioritized exclusion right, the exclusion being determined from the non-prioritized exclusion right information storage area, updating the information in the prioritized exclusion right information storage area to indicate that the prioritized information processing unit is trying to acquire the contended resource, the second process executing writes by using normal write instructions.*

Nowhere does Sadoi teach these elements. The first process of executing writes by using compare-and-swap instructions is performed on the a non-prioritized exclusion right information storage area and the second process executing writes by using normal write instructions is performed on the prioritized exclusion right information storage area, which are two separate and distinct storage areas. Accordingly, the presently claimed invention distinguishes over Zolnowsky alone and/or in combination with Sadoi for at least these reasons.

Claims 15 and 19 recite similar to claim 1. Therefore, the arguments are remarks made above with respect to claim 1 are also applicable to claims 15 and 19 and will not be repeated.

For the foregoing reasons, 1, 15, and 19 distinguish over Zolnowsky alone and/or in combination with Sadoi. Claims 2-13, 17, and 21-14 depend from claims 1, 15, and 19, respectively. Since dependent claims include all the limitations of the independent claims, claims 2-13, 17, and 21-14 distinguish over Zolnowsky alone and/or in combination with Sadoi, as well. Accordingly, Applicants believe that the rejection under 35 U.S.C. § 103(a) has been overcome and respectfully request that this rejection be withdrawn.

Conclusion

The foregoing is submitted as full and complete response to the Office Action mailed June 29, 2007 and it is submitted that claims 1-13, 15, 17, 19, and 21-24 are in condition for allowance. Reconsideration of the rejection is requested. Allowance of claims 1-13, 15, 17, 19, and 21-24 is earnestly solicited.

No amendment made was related to the statutory requirements of patentability unless expressly stated herein. No amendment made was for the purpose of narrowing the scope of any claim, unless the Applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

The Applicants acknowledge the continuing duty of candor and good faith to disclose information known to be material to the examination of this application. In accordance with 37 CFR §1.56, all such information is dutifully made of record. The foreseeable equivalents of any territory surrendered by amendment are limited to the territory taught by the information of record. No other territory afforded by the doctrine of equivalents is knowingly surrendered and everything else is unforeseeable at the time of this amendment by the Applicants and their attorneys.

The present application, after entry of this response, comprises twenty (20) claims, including three (3) independent claims. The Applicants have previously paid for twenty-six (26) claims including six (6) independent claims. The Applicants, therefore, believe that a fee for claims amendment is currently not due.

If the Examiner believes that there are any informalities that can be corrected by Examiner's amendment, or that in any way it would help expedite the prosecution of the patent application, a telephone call to the undersigned at (561) 989-9811 is respectfully solicited.

The Commissioner is hereby authorized to charge any fees that may be required or credit any overpayment to Deposit Account 50-0510.

In view of the preceding discussion, it is submitted that the claims are in condition for allowance. Reconsideration and re-examination is requested.

Respectfully submitted,

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